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EXAMINER	
VU, TRISHA U	

ART UNIT	PAPER NUMBER
2112	10

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/385,978	LEE ET AL.	
	Examiner	Art Unit	
	Trisha U. Vu	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *Amendment filed 10-30-03* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29,31-42* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29,31-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-29 and 31-42 are presented for examination.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-10 and 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over James et al. (5,841,989) (herein after James) in view of Tomizawa et al. (6,202,082) (herein after Tomizawa).

As to claim 1, James teaches a method of communicating between a plurality of functional blocks comprising: originating a packet (by a producer); passing the packet (each node is capable of passing by any packets that are not targeted for that node) (col. 5, lines 6-10). However, James does not explicitly disclose decoding the packet to extract configuration information from the packet and utilizing the configuration information to configure one of the plurality of functional blocks. Tomizawa teaches decoding configuration information packets to extract configuration information from the packet and utilizing the configuration information to configure one of the plurality of nodes (col. 20, lines 36-53, col. 22, lines 65-67, and col. 23, lines 1-6). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include configuration information packets as taught by Tomizawa in the system of James

to allow each node to know the system configuration of the ring, provide simple and high-speed network management and node condition management, and obviate the need to have a plurality of control packets (col. 22, lines 65-67 and col. 23, lines 1-6).

As to claim 2, James further teaches originating is performed by a master (producer) (col. 2, lines 10-14).

As to claims 3, 4, James further teaches passing is performed by a first target, and decoding is performed by a first target (col. 5, lines 5-10 wherein multicast and broadcast packets imply that a first target receives/decodes the packet and passes the packet to other targeted nodes).

As to claims 5, 6, James further teaches decoding is performed by a second target, and passing is performed by the second target (col. 5, lines 5-10 wherein multicast and broadcast packets imply that a second target receives/decodes the packet and passes the packet to other targeted nodes).

As to claim 7, James further teaches utilizing is performed by the second target (col. 2, lines 3-15) and passing is performed by the second target (col. 25, lines 5-10 wherein multicast and broadcast packets imply that the second target passes the packet to other targeted nodes).

As to claim 8, James further teaches removing the packet (aged packets are discarded when they pass through the scrubber) (col. 6, lines 23-26).

As to claim 9, James further teaches the first target comprising a ring interface and a control, the second target comprising a ring interface and a control, the master comprising a ring interface and a control, a ring connecting to the ring interface of the

first target, the ring interface of the second target, and the ring interface of the master in a daisy chain fashion, the ring used for the passing and the originating (Figs. 4, 5, 7 for interface connection between the nodes wherein node1 can be the first master and subsequent nodes can be targets, and col. 9, lines 17-21 wherein a control in each of the nodes can be at least a transmit unit 250 and/or a receive unit 252 with scrubber 218).

As to claim 10, James further teaches the master performing the removing after the passing brings the packet back to the master (col. 6, lines 23-26 and col. 40-44 wherein a scrubber for removing aged packets preferably is available within all of the nodes, and thus it can be implemented at the master node).

As to claim 17, James teaches a communications network comprising: a first master having a ring interface and a control; a first target having a ring interface and a first decoder; a first ring connection coupling the ring interface of the first master to the ring interface of the first target; a second target having a ring interface and a second decoder; and a second ring connection coupling the ring interface of the first target to the ring interface of the second target to pass a first plurality of packets; and a third ring connection coupling the ring interface of the second target to the ring interface of the first master to pass a second plurality of packets (Figs. 4, 5, 7 for interface connection between the nodes wherein node1 can be the first master and subsequent nodes can be targets, and col. 9, lines 17-21 wherein a control in each of the nodes can be at least a transmit unit 250 and/or a receive unit 252 with scrubber 218). However, James does not explicitly disclose configuration information packets to configure the nodes. Tomizawa teaches configuration information packets to configure nodes (col. 20, lines 36-53, col.

22, lines 65-67, and col. 23, lines 1-6). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include configuration information packets as taught by Tomizawa in the system of James to allow each node to know the system configuration of the ring, provide simple and high-speed network management and node condition management, and obviate the need to have a plurality of control packets (col. 22, lines 65-67 and col. 23, lines 1-6).

As to claim 18, James further teaches the master originates the plurality of packets which are passed via the first ring connection to the first target (each node is capable of passing by any packets that are not targeted for that node) (col. 5, lines 6-10).

As to claim 19, James further teaches the first target passed the plurality of packets via the second ring connection to the second target; and the second target passes the set of packets via the third ring connection to the first master (each node is capable of passing by any packets that are not targeted for that node) (col. 5, lines 6-10).

As to claim 20, the argument above for claim 19 applies. However, James does not explicitly teach the first target comprises a first configuration block on an integrated circuit; and the second target comprises a second configuration block on the integrated circuit. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the first and second targets to comprise a first and second configuration block on the integrated circuit since it has been held that forming in one piece an article which has formerly been formed in two pieces and put together involves only routine skill in the art. *Howard v. Detroit Stove Works,* 150 U.S. 164 (1893).

3. Claims 11-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over James et al. (5,841,989) (herein after James) in view of Tomizawa et al. (6,202,082) (herein after Tomizawa) as applied to claim 1 above, and further in view of Christiansen et al. (5,983,302) (herein after Christiansen).

As to claim 11, James further teaches a ring used for the originating and the passing (col. 3, lines 5-10). However, James and Tomizawa do not explicitly disclose requesting the ring and granting the ring. Christiansen further teaches requesting and granting a shared bus (col. 5, lines 26-50). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include requesting and granting the shared bus as taught by Christiansen in the ring system of James and Tomizawa to provide a computer system wherein the control of a shared bus by a plurality of devices include in the computer system is provided in a manner whereby overall operating efficiency is enhanced without effectively denying one or more devices in the computer system form control of the bus for extended periods of time (col. 2, lines 49-54).

As to claim 12, James further teaches the originating is performed by a first master (col. 2, lines 10-14).

As to claim 13, Christiansen further teaches the requesting is performed by a second master (col. 5, lines 34-56).

As to claim 14, Christiansen further teaches the granting is performed by the first master (by arbiter 22) (col. 5, lines 17-33 wherein arbiter 22 can be located anywhere throughout the computer system, thus it can be located as part of a first master device).

As to claim 15, Christiansen further teaches the granting is performed by an arbiter (by arbiter 22) (col. 5, lines 17-33).

As to claim 16, Christiansen further teaches arbitrating between a first master requesting the ring and a second master requesting the ring (col. 5, lines 50-56).

4. Claims 21-25, 27-29, 31-35, and 37-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over James et al. (5,841,989) (herein after James) in view of Christiansen et al. (5,983,302) (herein after Christiansen) and PCI Local Bus Specification (Herein after PCI Spec), and further in view of in view of Tomizawa et al. (6,202,082) (herein after Tomizawa).

As to claim 21, James teaches a communications network comprising: a first master; a first target; a second target; and a ring coupled to the first master, the first target, the second target (Figs. 4, 5 for ring connection between the nodes wherein node1 can be the first master and subsequent nodes can be targets). However, James does not explicitly disclose the ring comprising a packet valid line configured to indicate whether a valid packet is being transmitted on the ring. Christiansen teaches a packet valid line (FRAME# line) configured to indicate whether a valid packet is being transmitted on the ring (note Fig. 2 wherein a PCI local bus is provided for transmitting data between requesting devices, thus FRAME# line is inherent in PCI local bus). PCI Spec is being provided as evidence that a PCI local bus comprises a FRAME# line. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include PCI local bus with a packet valid line as taught by Christiansen in the ring system of James because PCI bus provides high communication speed. However, James and

Christiansen do not explicitly disclose configuration information packets to configure the nodes. Tomizawa teaches configuration information packets to configure nodes (col. 20, lines 36-53, col. 22, lines 65-67, and col. 23, lines 1-6). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include configuration information packets as taught by Tomizawa in the system of James and Christiansen to allow each node to know the system configuration of the ring, provide simple and high-speed network management and node condition management, and obviate the need to have a plurality of control packets (col. 22, lines 65-67 and col. 23, lines 1-6).

As to claim 22, James further teaches a second master, the ring coupled to the second master (Figs. 4, 5 and col. 5, lines 5-10 wherein node1 can be the first master and one of the subsequent nodes can be the second master).

As to claim 23, James does not explicitly disclose an arbitrator, the arbitrator coupled to the first mater, the arbitrator coupled to the second master, the arbitrator controlling activity of the first master and the second master. Christiansen teaches an arbitrator coupled to requesting devices, the arbitrator controlling activity of the requesting devices (col. 5, lines 26-50). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include an arbitrator coupling to the requesting devices and controlling the activity of requesting devices as taught by Christiansen in the ring system of James to provide a computer system wherein the control of a shared bus by a plurality of devices include in the computer system is provided in a manner whereby overall operating efficiency is enhanced without

effectively denying one or more devices in the computer system form control of the bus for extended periods of time (col. 2, lines 49-54).

As to claim 24, Christiansen further teaches a request line (request line 28), the request line coupled to the first master, the request line coupled to the second master (requesting devices); and a grant line (grant line 30), the grant line coupled to the first master, the grant line coupled to the second master (Fig. 2).

As to claim 25, Christiansen further teaches the request line configured to pass signals in a first direction, the grant line configured to pass signals in a second direction (Fig. 2).

As to claim 27, James does not explicitly disclose a request line, the request line coupled to the first master, the request line coupled to the second master, the request line coupled to the first target, the request line coupled to the second target. Christiansen teaches a request line coupled to requesting devices (col. 5, lines 26-50). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a request line coupling to the requesting devices as taught by Christiansen in the ring system of James to provide a computer system wherein the control of a shared bus by a plurality of devices include in the computer system is provided in a manner whereby overall operating efficiency is enhanced without effectively denying one or more devices in the computer system form control of the bus for extended periods of time (col. 2, lines 49-54).

As to claim 28, Christiansen further teaches the request line configured such that signals flow in a logically opposite direction to signals on the ring (Fig. 2).

As to claim 29, James further teaches a set of data lines configured to transmit signals (bus to transmit packet) (col. 2, lines 7-11). However, James does not explicitly teach a grant line. Christiansen further teaches a grant line configured to indicate a master may use the ring (grant line 30) (Fig. 2).

As to claim 31, James further teaches the ring comprising a set of data lines, the data lines configured to transmit signals (bus to transmit packet) (col. 2, lines 7-11).

As to claim 32, James further teaches the first master utilizing the ring to transmit signals to the first target, the first target utilizing the ring to transmit signals to the second target, the second target utilizing the ring to transmit signals to the first master (col. 5, lines 1-9).

As to claim 33, James further teaches the first master comprising a ring interface coupled to the ring and a control coupled to the ring interface, the control suitable for generating packets, the packets transmitted through the ring interface to become signals on the ring (Figs. 4, 5, 7 for interface connection between the nodes, and col. 8, lines 34-54 wherein the control can be at least a transmit unit 250).

As to claim 34, James further teaches the first target comprising a ring interface and a decoder coupled to the ring interface, the decoder receiving the signals that represent a packet (receive unit 252) (Figs. 4, 5, 7 for interface connection between the nodes), the decoder determining if the packet is addressed to the first target (by TargetID field 92 of the packet as shown in Fig. 2).

As to claim 35, James further teaches the second target comprising a ring interface and a decoder coupled to the ring interface, the decoder receiving the signals

that represent a packet (receive unit 252) (Figs. 4, 5, 7 for interface connection between the nodes), the decoder determining if the packet is addressed to the second target (by TargetID field 92 of the packet as shown in Fig. 2).

As to claim 37, James further teaches the packet comprised of a fixed number of units of data, the units of data encoding an address (TargetID and/or SourceID) (col. 1, lines 41-44 and col. 5, lines 51-64).

As to claim 38, James does not explicitly teach the first master, the first target and the second target on an integrated circuit. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the first and second targets to comprise a first and second configuration block on the integrated circuit since it has been held that forming in one piece an article which has formerly been formed in two pieces and put together involves only routine skill in the art. *Howard v. Detroit Stove Works,* 150 U.S. 164 (1893).

As to claim 39, James does not explicitly teach the first master and the first target on a first integrated circuit, the second target on a second integrated circuit. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the first and second targets to comprise a first and second configuration block on the integrated circuit since it has been held that forming in one piece an article which has formerly been formed in two pieces and put together involves only routine skill in the art. *Howard v. Detroit Stove Works,* 150 U.S. 164 (1893).

As to claim 40, James does not explicitly teach the first master on a first integrated circuit, the first target and the second target on a second integrated circuit. It

would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the first and second targets to comprise a first and second configuration block on the integrated circuit since it has been held that forming in one piece an article which has formerly been formed in two pieces and put together involves only routine skill in the art. *Howard v. Detroit Stove Works,* 150 U.S. 164 (1893).

As to claim 41, James further teaches the second master comprising a buffer (elasticity buffers 222 and 224), the buffer utilized for storing incoming data when the second master originates a packet, the incoming data passed after the second master completes origination of the packet (Fig. 7 and col. 8, lines 34-45).

1. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over James et al. (5,841,989) (herein after James) in view of Christiansen et al. (5,983,302) (herein after Christiansen) and PCI Local Bus Specification (Herein after PCI Spec), further in view of Tomizawa et al. (6,202,082) (herein after Tomizawa) as applied to claim 25 above, and further in view of Desyllas et al. (4,697,268) (herein after Desyllas).

As to claim 26, James, Christiansen and Tomizawa do not explicitly teach the first direction and the second direction dynamically alterable. Desyllas teaches bus request/grant directions are dynamically alterable (col. 2, lines 38-50 wherein bus request/grant lines are bi-directional lines for carrying request and grant signals in opposite direction, this implies that opposite directions are dynamically alterable since the lines are bi-directional lines). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include bi-directional request/grant lines

(dynamically alterable request/grant directions) as taught by Desyllas in the system of James, Christiansen and Tomizawa to provide alternate path for data transmission and thus improve the system's speed.

2. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over James et al. (5,841,989) (herein after James) in view of Christiansen et al. (5,983,302) (herein after Christiansen) and PCI Local Bus Specification (Herein after PCI Spec), further in view Tomizawa et al. (6,202,082) (herein after Tomizawa) as applied to claim 35 above, and further in view of Hartmann et al. (6,047,002).

As to claim 36, James further teaches the packet comprised of a header and a set of data (Fig. 2 and col. 12, lines 46-67). However, James does not explicitly teach the header including an indication of the logical size of the set of data. Hartmann teaches a header including an indication of the logical size of the set of data (data length field (col. 11, lines 50-57). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a header including an indication of the logical size of the set of data as taught by Hartmann in the system of James, Christiansen and Tomizawa to provide the system with the ability to transmit packets of different sizes wherein the data size field helps the receive unit to better utilize its buffer to store data.

3. Claim 42 is rejected under 35 U.S.C. 103(a) as being unpatentable over Szczepanek (5,374,926) in view of Tomizawa et al. (6,202,082) (herein after Tomizawa)

As to claim 42, Szczepanek teaches a system comprising: a processor (communication processor 11); a processor bus coupled to the processor (bus 16); a data chip coupled to the processor bus (RAM 14); and an address chip coupled to the processor bus and coupled to the data chip (external address compass logic 10, protocol handler 12, and/or ring I/F 9); the address chip including a configuration ring (through ring interface 9), the configuration ring having a master, a first target and a second target, the master coupled through a ring to the first target, the first target coupled through the ring to the second target, the second target coupled through the ring to the master (Figs. 1 and 2). However, Szczepanek does not explicitly disclose configuration information packets to configure the first and second targets. Tomizawa teaches configuration information packets to configure nodes (col. 20, lines 36-53, col. 22, lines 65-67, and col. 23, lines 1-6). It would have been obvious to one of ordinary skill in the art at the time the invention was made to include configuration information packets as taught by Tomizawa in the system of Szczepanek to allow each node to know the system configuration of the ring, provide simple and high-speed network management and node condition management, and obviate the need to have a plurality of control packets (col. 22, lines 65-67 and col. 23, lines 1-6).

Response to Arguments

4. Applicant's arguments, filed 10-30-03, with respect to the newly added limitation "configuration information to configure the functional blocks" in claim(s) 1, 17, 21, and 42 have

been fully considered and are persuasive. Upon further consideration, a new ground(s) of rejection is made in view of newly found prior art reference(s).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Trisha U. Vu whose telephone number is 703-305-5959. The examiner can normally be reached on Mon-Thur and alternate Fri from 7:00am to 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Trisha Vu

Trisha U. Vu
Examiner
Art Unit 2112

uv

Sumati Lefkowitz

SUMATI LEFKOWITZ
PRIMARY EXAMINER